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Design and Implementation of ECG Signal Acquisition and Processing System Based on FPGA

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ABSTRACT

At present, ECG is an important basis for detecting and judging cardiovascular disease. The ECG signal processing level directly determines the accuracy of diagnosis of this disease. With the increasing demand of human society for the accuracy and timeliness of ECG signal processing, the current conventional processing methods no longer meet the need for precision, so it is necessary to adopt more accurate algorithm processing and more rapid algorithm implementation. Aiming at this trend, a FPGA-based ECG signal acquisition and processing system is designed. The system takes FPGA as the control center, realizes the digital-to-analog conversion through a D conversion module, realizes the high-order digital filtering with the FIR filtering algorithm, the data obtained is transmitted to the computer through the serial port, and finally is displayed, to facilitate the initial self-diagnosis of heart disease patients.

1. Introduction

Cardiac diseases mainly include myocardial infarction, myocardial ischemia, atrial flutter and ventricular tachycardia, which have the characteristics of paroxysmal and high risk. With the improvement of People's living standard and health consciousness, the demand for real-time monitoring of heart diseases is also increasing. ECG is a kind of bioelectric signal produced by myocardial contraction and can provide information of cardiac physiological function changes. The analysis and diagnosis of ECG has become an important means to detect heart diseases.

Since the first ECG machine was used in clinic in 1906, the ECG monitoring system can be divided into three types: ECG machine, ECG instrument and wearable ECG acquisition system. In recent years, with the development of digital signal processing technology and the appearance of tablet computer and large-screen smartphone, ECG monitor is becoming more portable, more cost-effective and more intelligent.

Most of the current ECG signal acquisition devices use dual-CPU structure, the disadvantages of which are poor coordination, large power consumption and volume, low stability, because the FPGA device has the characteristics of low power consumption, high performance, low cost and parallel processing structure, the utility model can well meet the requirements of the portable ECG acquisition instrument, such as high processing speed, low power consumption, small volume, low price, strong stability, and portable etc.

2. System architecture

ECG signal acquisition and processing system structure as shown in Fig 1, the system mainly AD8232 signal acquisition, FPGA storage and processing, C # GUI display and MATLAB processing. FPGA processing is the core part, which consists of the following modules: AD module, Filter Module, RAM module, and UART module.

The FPGA is powered by the Xilinx Artix-7 series chip xc7a35tcpg236-1. XADC has two special differential input pins, Vp and Vn, which can be used to sample analog signals. Data sampling from 100MHz to 360Hz is accomplished by ADC module, the low-pass filter is also used to eliminate common mode noise; after all memory cells are filled with ECG sample data, a pulse is generated to trigger the transmission to the PC. The UART module will receive a signal, which is sent using the TX module, and when the receiving UART detects the start bit, it will start reading the input bit at a

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specific frequency called the baud rate.

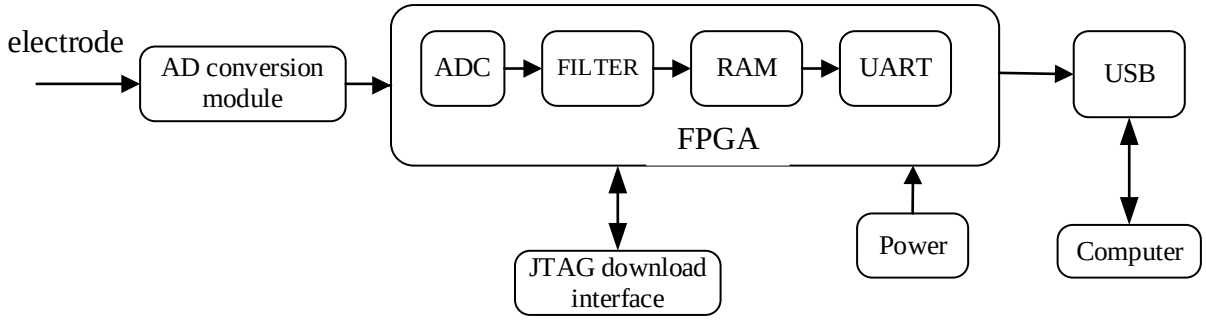

Fig 1 System structure diagram

3. FPGA digital system design

FPGA digital system mainly includes SPI module, Central Logic Module, Digital filter module, input buffer module, output buffer module, 8-bit data to 24-bit data 8to24bit module and USB interface module.

SPI interface module is responsible for communication with AD8232, SPI interface module can be written according to the standard SPI protocol. SPI consists of 4 signal lines: Clock SCLK, selected CS, data output MOSI and data input miso. Xilinx's 7 series FPGA and Zynq devices creatively integrate Analog-to-digital converter and related on-chip sensors (built-in temperature and power sensors) into the chip, allowing XADC to directly capture some of the power supply voltage of the chip junction and the FPGA, used to monitor the internal state of the FPGA. It also provides 17 pairs of differential pins, one pair of dedicated analog differential inputs and 16 pairs of reusable analog differential inputs, which can be used as ordinary UserI/O when not in use. In addition to the FPGA internal temperature and various voltage monitoring, but also reuse a 12bit ADC conversion, in which the reference voltage can be internal 1.25 V, or external stable reference voltage source. After the conversion, there is a control register and a state register, which can be connected to the FPGA's internal logic through the FPGA's DRP interface.

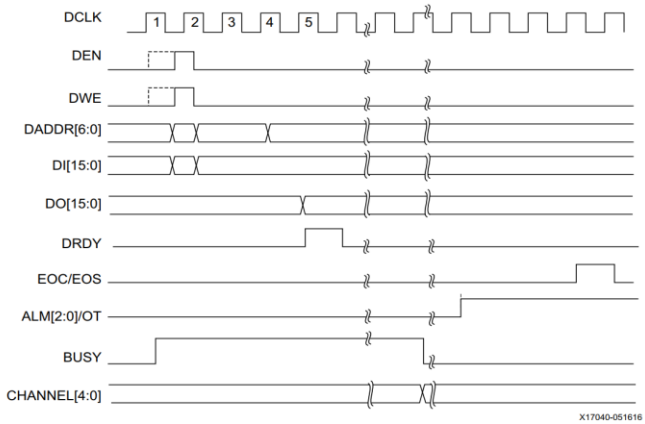

Fig 2 sequence diagram of the DRP interface

The DRP interface sequence diagram is shown Fig 2. When the DEN signal is pulled up, the input data DI and the input address DADDR bus are received by the internal XADC; the DWE is pulled up to specify registers to write data to the internal XADC; and the DWE is pulled down to indicate that the current data is read, it returns drdy after several clock cycles. This DRDY is raised to indicate that the XADC internal register address, such as the VP/VN conversion value, is stored in the 03H address and reads the VP/VN register address data, which is the digital value of the voltage conversion, the data bus DO_OUT is stored in the ADC_OUT register.

3.1 ADC module

This part mainly consists of PLL, XADC, XADC module, XADC module completes AD sampling from 100mhz to 360hz. See Fig 3.

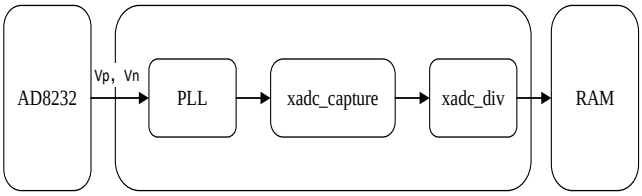

Fig 3 ADC module

In this circuit, the PLL is used to divide the input frequency (100 MHz-RRB- into 14 MHz, which is the frequency of XADCXADC input. Using the Clocking Wizard IP core, and the module has been connected to: CLK: Input Frequency (100mhz), CLK: Dynamic Reconfiguration Port Clock Input (XADC input).

XADC: XADC has two dedicated differential input pins, VP and VN, which can be used to sample analog signals. You can also use 16 secondary inputs. However, the FRBW (full resolution bandwidth) of these auxiliary inputs is lower at 250 kHZ, while the FRBW of dedicated inputs is 500 kHZ. Therefore, if we want to process signals near the maximum Nyquist frequency of the XADC, we need to use its dedicated input. The XADC can sample channels at speeds up to 1Msamples/SEC. Because XADC has a 12-bit resolution, we need the voltage across the capacitor to be stabilized within the LSB of the 12-bit value.

In the development board in use, the output of the electrode will be connected to the pin VAUX6, the analog voltage from the AD8232 will be converted to a digital signal, and the XADC is configured with a sample frequency of 36KSPS because the sample frequency of the database is 360Hz, the required input DCLK frequency (MHz) obtained from the PLL is 14 MHz for subsequent frequency division operations.

The simulation results are shown in Figure 4.

Fig 4 ADC simulation results

3.2 Low-pass filter

Digital filter is widely used in a variety of digital signal processing systems, it is in accordance with the design of the program, a group of input digital signals through certain operations into another group of output digital signals, in order to change the form and content of digital signal, to achieve the effect of signal filtering or processing[5]. According to the impulse response, the Digital filter can be divided into FIR (finite impulse response-RRB- filters IIR (infinite impulse response) filters. FIR filters are widely used because of their stability. In this paper, FIR algorithm is used to filter the digital ECG signal after A/D conversion.

The input signal is usually sampled by a Analog-to-digital converter and then Digital filter by a microprocessor and some peripheral components (such as memory for storing data and filter coefficients). Finally, a digital-to-analog converter completes the output phase. The program instructions (software) running on the microprocessor perform the necessary mathematical operations on the numbers received from the ADC to Digital filter. In some high-performance applications, use FPGA or ASIC instead of general-purpose microprocessors or dedicated DPS with specific parallel architectures to speed up operations such as filtering. A low-pass filter is a filter that passes through a signal at a frequency below a cut off frequency and attenuates a signal above that cut off frequency.

The unit impulse response of FIR filters is:

$$y(n) = \sum_{k=0}^{N-1} h(x)x(n-k) \tag{1}$$

The system transfer function of the FIR filter is:

$$H(Z) = \frac{Y(Z)}{X(Z)} = \sum_{n=0}^{N-1} h(k)Z^{-K} \tag{2}$$

Among them, $x(n)$is the sequence of input signals;$y(n)$ is the output signal sequence; $h(k)$ is the filter coefficient. The transformation of impulse response $h(n)$ of FIR digital filter is:

$$H(z) = \sum_{n=0}^{N-1} h(n)Z^{-n} \tag{3}$$

You can also write:

$$H(z) = h(0) + h(1)z^{-1} + \cdots + h(N-1)z^{-(N-1)} \tag{4}$$

From equation (1) , The output $\boldsymbol{y}(\boldsymbol{n})$ of a FIR filter of length N is equal to the system unit impulse response coefficient $\boldsymbol{h(k)(k = 0,1,2 \ldots N)}$ Finite convolution with the input time series $\boldsymbol{x(n)}$,The diagram is shown in Fig. 5. This structure is called the convolution structure of the FIR filter, also known as the immediate structure.

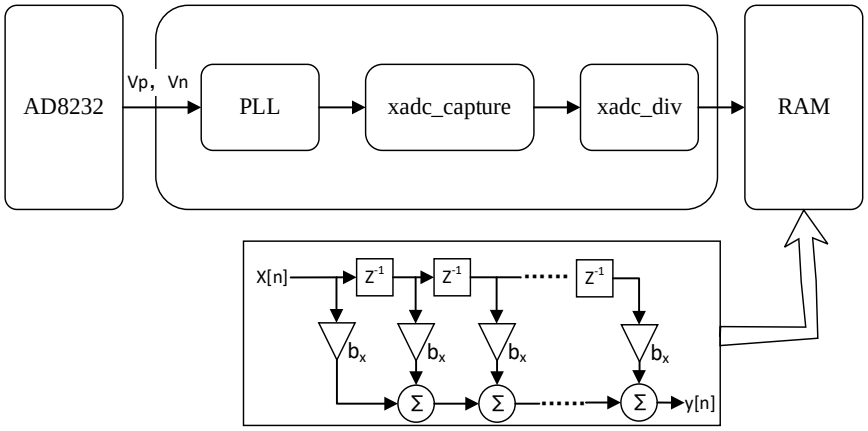

Fig 5 Convolution structure of FIR filter

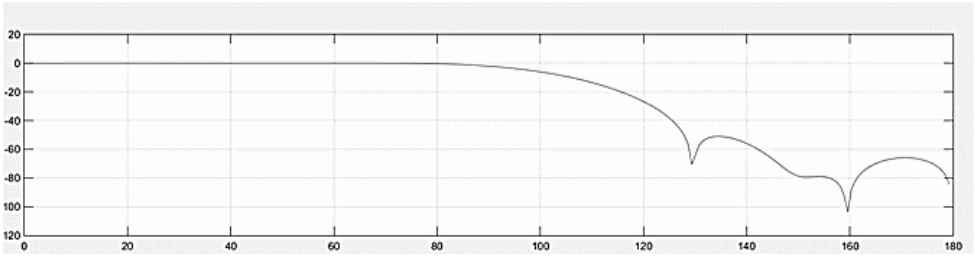

Fig 6 100 Hz low-pass filter

The program instructions running on the microprocessor perform the necessary mathematical operations on the numbers received from the ADC to Digital filter. In some high-performance applications, FPGA or ASIC are used instead of general-purpose microprocessors or dedicated DSPS with specific parallel architectures to speed up operations such as filtering. A low-pass

filter is a filter that passes through a signal at a frequency below a cut off frequency and attenuates a signal above that cut off frequency.

Filter part is mainly designed to Fir Verilog design, The module implements a 21st order ECG low-pass filter at 100hz to eliminate the noise in the ECG signal.

Filter design using Filter Designer in MATLAB, Results such as Fig 6.

Get the filter factor:

0	-3	-4	7	20	0	-52	-51	85	296	400	296	85	-51	-52	0	20

Figure shows the specific structure of the FIR filter.

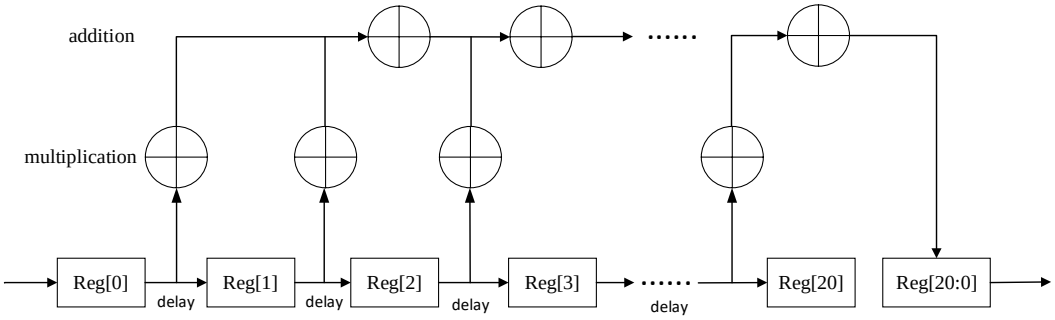

Fig 7 pipeline operation

Reg signed [9:0] prev[20:0] reg signed [9:0] prev[20:0]; And then the rest of the data as it comes in, it shifts in order.

In the case of the multiplicator filter coefficients, a multiplier IP core is invoked. 20 adders are used to add up the result of the product and the result is the filtered signal. The multiplier configuration interface is shown in Fig 8.

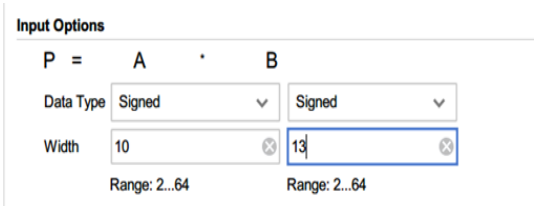

Fig 8 multiplier configuration interface

At present, the amount of ECG data that needs to be stored and processed is very large. In order to store the data effectively, data compression technology is needed. The main goal of ECG data compression is to obtain the highest compression ratio with the minimum loss of ECG useful information. Since 1960s, many ECG data compression methods have been proposed. These methods can be divided into three categories: direct compression, transform compression and characteristic parameter extraction. The research shows that LADT method has the best performance, small computation and good data recovery performance among the existing piecewise broken line fitting methods. Therefore,

This algorithm is selected for the ECG data compression algorithm in this paper. At present, the high-quality real-time ECG data compression can not be realized by the general SCM, so FPGA with high speed and high precision is used to realize the real-time ECG data compression. The experimental results show that the results are satisfactory.

The fitting process of LADT compression method is shown in the Fig 9. If F(i) is the starting point of a broken line and E(i +1) is the candidate end point, then

$$\theta_1 = \arctan\left[\frac{E(i+j)-E(i)}{j}\cdot T\right] \tag{5}$$

$$\theta_2 = \arctan\left[\frac{E(i+j)-E(i)}{k}\cdot T\right] \tag{6}$$

The distance from each point to the broken line can then be calculated by the following formula

$$d_i = \frac{|j\cdot Tsin(\theta_2-\theta_1)|}{|\cos\theta_1|} \tag{7}$$

Where, T is the sampling time:

$$d_{jmax} = \max(d_j) = E(i+j_{max}) \tag{8}$$

If $d_{jmax} > \varepsilon$ the fitting is not successful and the above process is repeated with E(i+j_{max}) as the end point until$d_{jmax} < \varepsilon$, otherwise the fitting is successful. E(i+k) and E(i+k) as the new starting point are recorded to start fitting another curve. Since trigonometric and inverse trigonometric functions need to be calculated, it cannot be directly realized in real time according to the above formula. In order to achieve real-time data compression, it puts forward the LADT rapid implementation method, it is thought through other ways to avoid the calculation of trigonometric function, in other literature has given the derivation process of the concrete, so, here only give a conclusion, its realization way is through the type to calculate the distance of each point to the line.

$$d_j^2 = \frac{\{j[E(i+k)-E(j)]-k[E(i+k)-E(j)]\}T^2}{[E(i+k)-E(i)]^2+k^2T^2} \tag{9}$$

To compare d_j ,j=1,2... , the relation between k and ε, Just compare the size relation between d_j^2 and ε^2, Because when a,b>0, $a^2 > b^2$. So desirable D =max(d_j^2),j=1, 2, ...,k, D< ε^2,the fitting is successful, otherwise, the fitting fails, so the LADT compression method is realized, and the square root calculation d_j is avoided, so the complex trigonometric function calculation is avoided. It makes it possible to implement the LADT algorithm in real time by FPGA.

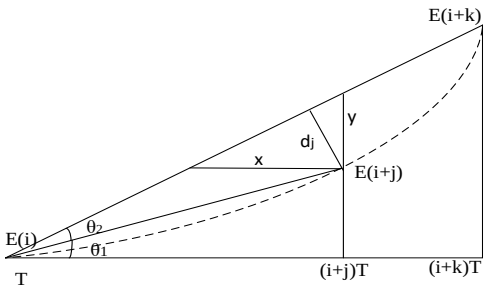

Fig 9 LADTarithmetic

3.3 RAM module

Need to store ADC samples, so the use of RAM, RAM is commonly used in FPGA basic module, can be widely used in the case of cache data, it is also the basis of Rom, FIFO. On-chip Ram has two command modes: read and write. Both of these states are controlled by WE signals that are high when write mode is enabled and low when write mode is disabled.

The Reg Signal of [11:0] memory [0:2048] is used here. For each trigger pulse, the index is incremented and a sample is stored. When the index is 2048, a pulse is generated and the system changes its state, and then the RAM is in full read mode.

After the ram cell is full of ECG sample data, a pulse PULSEMEM will be generated to trigger the transmission to the PC, and the UART module will receive the signal (the signal will be allowed to be sent using the TX module) , this pulse also controls the data flow and is not sent in incomplete data, which can slow down the obtained results and operate on subsequent state machines.

The simulation results are as follows. As can be seen from the figure, data_in data is written to address 0 at 2049, and in the last cycle, that is, data_out data is 1, indicating that valid data is read out, and there is a memory_delay for the whole write and read.

3.4UART modules

The baud rate is the maximum number of bits transmitted per second, including starting bits, data bits, parity bits, and stop bits. If the baud rate is set to 9600, then the length of a bit of data is 19600 sec. The baud rate in this experiment is generated by a 100MHz clock.

Through the state machine design UART, in the UART communication, two UART direct communication. UART_TX converts the parallel data into serial form, sends it serial to UART_RX, and UART_RX converts the received serial data into parallel data. Only two lines are needed to transfer data between two UARTS. Data from Tx pin of UART_TX to Rx pin of UART_RX.

Taking the UART module as an example, here is the timing diagram of the control signal interface. The simulation results are shown in Figure 10.

The baud rate in this experiment is generated by the 100MHz clock, and the serial port communication baud rate is 9600. According to Formula 10, the serial port transmits 1 data bit every 10416 clock cycles.

$$P = \frac{\frac{1}{9600}\cdot 10^{9}}{10ns} = 10416 \quad (10)$$

At S0, the system is idle and data needs to be raised. The BUSY signal is a flag signal that is being sent by the serial port. BIT_POS is a counting operation for each data bit. It is mainly used to detect a signal of the module to be sent, where the EN signal is detected and the S1 state is entered.

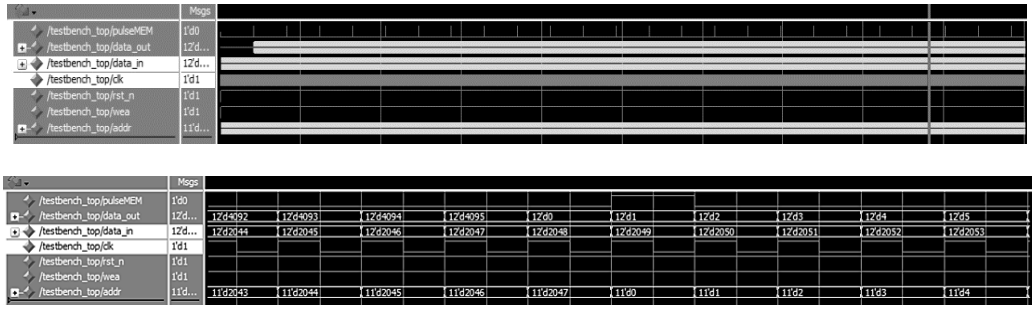

Fig 10 ram Simulation

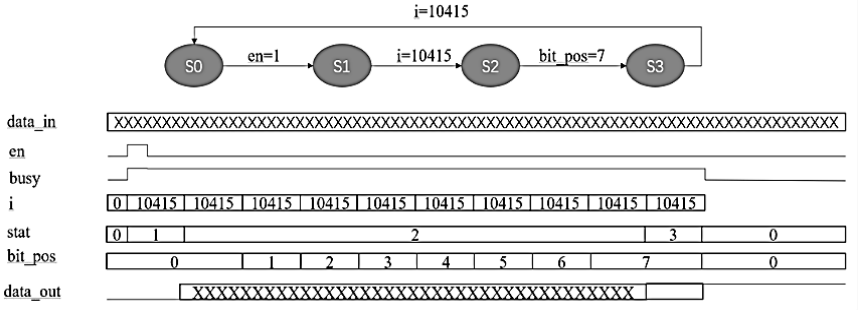

Fig 11 Control signal interface timing diagram

At S1, when I is at its maximum, and you can see here that I is 10415, this DATA_OUT is going to pull down, which means that at the start bit S2, BIT_POS is going to count from 0 to 7, and then the data is going to be transmitted, so after the start bit here, it's 55, which is 10101010, From the lowest to the highest.

At S3, the OUT is pulled up, and then the various control signals are zeroed out, including the counter, if not zeroed out, which affects the next transmission.

UART protocol principle: message frame from a low start bit, followed by 7 or 8 data bits, a usable parity bit and one or more high stop bit. When the receiver finds the start bit, it knows that the data is ready to be sent and tries to synchronize with the sender clock frequency. If parity is selected, the UART adds a parity bit after the data bit. Parity bits can be used to aid in error checking. In the receiving process, UART removes the start and end bits from the message frame, parity the incoming bytes, and converts the data bytes from serial to parallel. The UART transport timing looks like this Fig. 12:

UART asynchronously transmits data, which means that no clock signal synchronizes the UART's-bit output with the-bit sampling of the received UART. Send the UART instead of the clock signal to add the start and stop bits to the packet being transmitted. These bits define the start and end of the packet, so the receiving UART knows when to start reading them.

When the receiving UART detects the start bit, it begins to read the input bit at a specific frequency called the baud rate. The baud rate is a measure of the speed at which data is transmitted, expressed as BPS. The two UART's have to work at roughly the same baud rate. The baud rate difference between sending and receiving UART is only about 10% before the timing of the bits gets too far out.

The module also has a good synchronization method: the START control signal, only when the pin is high, will start to send. You also need to check whether the flag is busy-whether another transmission is going on, and TXDONE is the flag that signals when the transmission is executing.

The UART block reads the cache sample one by one and sends it to the PC, because the length of the UART packet is 8 bits, so each sample is divided into two bytes. As shown in the diagram.

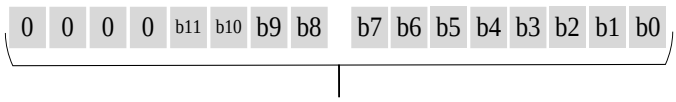

Fig 12 AD (12 bit) capture to send (8 bit)

Because the ADC only has 12 bits, and the UART only has 8 bits, we need to transmit 2 sets of data, 8 bits on the even and even parity, and 4 bits on the odd and even parity.

4. Experimental results

4.1 Integrated design

The upper computer collects the result.The PC C # program is designed to connect to the FPGA via the UART. After downloading the bit stream to the FPGA and setting the amplifier on the electrodes, click the "Send"button in the GUI to start the collection. Then, with the "Get"button, the sample data is sent to the PC and displayed. The result is shown in Fig 15.

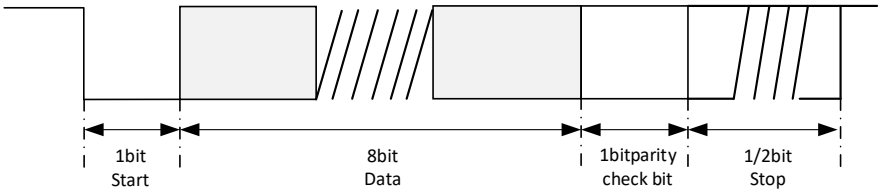

Fig 13 UART transport sequence diagram

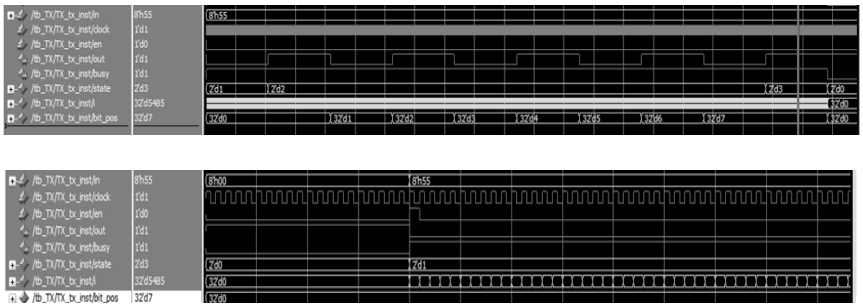

Fig 14 Verilog simulation verification

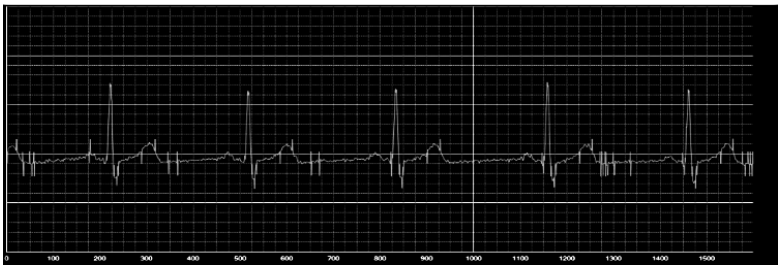

Fig 15 Graphical result

4.2 Performance evaluation

According to the comprehensive report, the system clock meets the design requirements. The usage rates of LUT, LUTRAM, FF, BUFG and MMCU were 10%, 5%, 2%, 13% and 20%, respectively. In addition, the total power consumption of the system is only W, with

lower system power consumption. The visualization results are shown in Figure 16.17.18.

5. Conclusion

The FPGA-based ECG signal acquisition and processing system is neither a substitute for medical consultation nor a cure for any disease, but a suitable system for examining the medical condition of the human body in a specific location. Such a project could be used to monitor the health of elderly patients who are unable to go to hospital or to check whether their condition has changed. The ECG signals from the electrodes are amplified using the AD8232(amplifier) and then sent to the Bays3 Development Board, where they are processed. The project also features a GUI (graphical user interface) developed in C # to display the ECG.

One of the biggest problems with this project is the transmission accuracy: because of the 12-bit ADC and the 8-bit UART, it's hard to resolve the differences without losing signal synchronization. But the problem is well solved by the many control signals between the modules.

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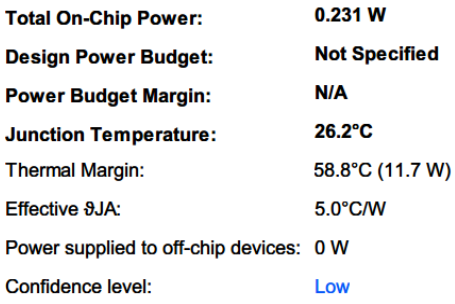

Fig 16 Resource consumption chart(1)

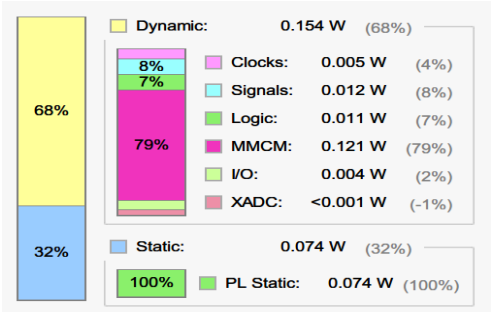

Fig 17 Resource consumption chart(2)

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	2082	20800	10.01
LUTRAM	512	9600	5.33
FF	884	41600	2.13
IO	11	106	10.38
BUFG	4	32	12.50
MMCM	1	5	20.00

Fig 18 Resource consumption table

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